On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs

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Presentation Outline

- Introduction
  - Why fault tolerance is critical?
  - Especially for the FPGA domain

- Motivation
  - Limitations of existing solutions

- Proposed methodology

- Experimental results

- Conclusions
Reconfigurable platforms are everywhere...

"On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs"
A problem has been detected and Windows has been shut down to prevent damage to your computer.

**DRIVER_IRQL_NOT_LESS_OR_EQUAL**

If this is the first time you've seen this Stop error screen, restart your computer. If this screen appears again, follow these steps:

Check to make sure any new hardware or software is properly installed. If this is a new installation, ask your hardware or software manufacturer for any Windows updates you might need.

If problems continue, disable or remove any newly installed hardware or software. Disable BIOS memory options such as caching or shadowing. If you need to use Safe Mode to remove or disable components, restart your computer, press F8 to select Advanced Startup Options, and then select Safe Mode.

Technical information:

*** STOP: 0x000000D1 (0x0000000C, 0x00000002, 0x00000000, 0xF86B5A89)

*** gv3.sys - Address F86B5A89 base at F86B5000, DateStamp 3dd991eb

Beginning dump of physical memory
Physical memory dump complete. Contact your system administrator or technical support group for further assistance.
A problem has been detected and windows has been shut down to prevent damage to your computer.

If anything can go wrong, it will

Murphy’s Law

If this is the first time you've seen this stop error screen, restart your computer. If this screen appears again, follow these steps:

Check to make sure any new hardware or software is properly installed. If this is a new installation, ask your hardware or software manufacturer for support.

If you or your systems administrator is unable to solve your problem, contact Microsoft Product Support Services.

*** STOP: 0x000000D1 (0x000000c, 0x00000002, 0x00000000, 0xF86B5A89)

*** gv3.sys - Address F86B5A89 base at F86B5000, DateStamp 3dd991eb

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*Murphy’s Law*

*** STOP: 0x000000D1 (0x0000000C, 0x00000002, 0x00000000, 0xF86B5A89)***

*** gvs.sys - Address F86B5A89 base at F86B5000, DateStamp 3dd991eb***

Beginning dump of physical memory
Physical memory dump complete.
“On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs”
What is “fault”? 

- A fault is the cause of the error 
- A system fails when it cannot meet its promises (specifications) 

How can we deal with problems? 
- Option 1: Make problems less likely 
- Option 2: Fail, but don’t corrupt anything 
- Option 3: Transparently tolerate problems 

Faults can be: 
- Transient (appear once and disappear) 
- Intermittent (appear-disappear-reappear behavior) 
- Permanent (appear and persist until repaired)
Failures start appearing much sooner

System-level failures appear much sooner during operation, reducing the system lifetime and jeopardizing lifetime specs

\[ MTTF = A \cdot j^{-n} \cdot e^{\frac{E_a}{k_B T}} \]
Failures start appearing much sooner

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\[ \text{MTTF} = A \cdot j^{-n} \cdot e^{\frac{E_a}{k_B T}} \]

"On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs"
The impact of SEU faults in FPGA

Faults are more crucial for FPGAs than ASICs

They can alter the design, not only the data

“On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs”
The 4 stages of fault-free architectures

- **Execution**
- **Monitoring**
- **Failure Detection**
- **Failure Repair**
"On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs"
“On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs”
Why temperature is critical?

- Power dissipation has peaked
- This becomes even more important with device scaling
- Higher power densities

"On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs"
Thermal stress: Initial vs. Xilinx TMR

Initial (without TMR)

Uniform TMR (e.g. Xilinx TMR)

(a)

(b)

0% – 20%  20% - 40%  40% - 60%  60% - 80%  80% - 100%

Minimum Temperature

Maximum Temperature

"On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs"
Locating Regions of Importance

The first step in order to build a reliable system is to identify possible regions with increased failure probability. These regions mostly include hardware resources that implement application’s functionalities with increased switching capacitance.

(based on switching capacitance) (based on temperature)

Target benchmark: DES (1,591 Slices) – The temperature profile derived from Hotspot
Locating Regions of Importance

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- These regions mostly include hardware resources that implement application’s functionalities with increased switching capacitance

(based on switching capacitance) (based on temperature)

Differences between estimation and simulation

(a)

(b)

The variation between these maps is only 126 slices (or about 8% of the total device slices)

"On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs"
The first step in order to build a reliable system is to identify possible regions with increased failure probability. These regions mostly include hardware resources that implement application’s functionalities with increased switching capacitance.

Target benchmark: DES (1591 Slices) – The temperature profile derived from Hotspot
Exploration space for game theory

![Graph showing exploration space for game theory with normalized PoF and EDP values, highlighting candidate solutions, selected solution, and optimal solutions for PoF and EDP reduction.]

- Optimal solution in term of PoF reduction: (PoF_H=1.00 & PoF_L=0.00)
- Optimal solution in term of EDP reduction: (PoF_H=0.50 & PoF_L=0.50)
- Selected solution: (PoF_H=0.66 & PoF_L=0.34)
- Candidate solutions
Proposed Framework

Insertion of TMR (e.g. [Xilinx2010]) → Synthesis (Quartus) → P&R (VPR)

Application (HDL)

Designer

Input/Output
Existing Software Tool
New Software Tool
Condition

“On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs”
Proposed Framework

Static Fault Tolerance

Design-Time

- Insertion of TMR (e.g. [Xilinx2010])
- Synthesis (Quartus)
- P&R (VPR)

Evaluation

- Fault injection tool (Fault-Inject)
- Selective elimination of TMR (Fault-Free)
- Calculate map with PoF values (Fault-Free)

Desired fault masking

Task to be solved with game theory

Application (HDL)

Current Software Tool

New Software Tool

Input/Output

Existing Software Tool

Condition

"On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs"
Proposed Framework

Design-Time

Application (HDL)

Static Fault Tolerance

Insertion of TMR (e.g. [Xilinx2010]) → Synthesis (Quartus) → P&R (VPR)

Evaluation

Acceptable solution?

Fault injection tool (Fault-Inject)

Selective elimination of TMR (Fault-Free)

Calculate map with PoF values (Fault-Free)

Desired fault masking

Task to be solved with game theory

No

Input/Output

Existing Software Tool

New Software Tool

Condition

On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs"
Proposed Framework

**Design-Time**
- Application (HDL)
- Insertion of TMR (e.g. [Xilinx2010])
- Synthesis (Quartus)
- P&R (VPR)
- Calculate map with PoF values (Fault-Free)
- Evaluation
- Fault injection tool (Fault-Inject)
- Selective elimination of TMR (Fault-Free)
- Desired fault masking
- Task to be solved with game theory
- Acceptable solution?

**Run-Time**
- Selectively enable/disable fault tolerance (Dagger)
- Update map with PoF values (Fault-Free)
- Compute map with PoF values (Fault-Free)
- Fault injection tool (Fault-Inject)
- Application execution

**Static Fault Tolerance**
- No
- Yes

**Dynamic Fault Tolerance**
- No
- Same?
- Yes

“On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs” 15
MEANDER Framework

http://proteas.microlab.ntua.gr

"On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs"
Architecture of a Virtual FPGA

- The underline hardware is a general-purpose conventional FPGA device.

- Additional technical details about the underline Virtual-FPGA architecture can be found in [1]

Application mapping under different fault tolerant scenarios

With TMR

“On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs”
Application mapping under different fault tolerant scenarios

With TMR

(a)

Without TMR

(b)
Application mapping under different fault tolerant scenarios

With TMR

Original functionality

Replica #1

Replica #2

Voter

(a)

Without TMR

Original functionality

Off

Off

Off

(b)

(c)

(d)

Original BLE (A)

Replica #1 (B)

Replica #2 (C)

Output (V)

A 0 0 0 0 1 1 1 1
B 0 0 1 1 0 0 1 1
C 0 1 0 1 0 1 0 1
V 0 0 0 1 0 1 1 1

"On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs"
Exploration space

- Maximum Operation Frequency (Timing-aware P&R [27], [37])
- Maximum Operation Frequency (Fault tolerant-aware P&R)
- Power Consumption (Timing-aware P&R [27], [37])
- Power Consumption (Fault tolerant-aware P&R)
Exploration space

acceptable solutions that meet performance specifications

Maximum affordable degradation in operation frequency

Maximum Operation Frequency (Timing-aware P&R [27], [37])

Maximum Operation Frequency (Fault tolerant-aware P&R)

Power Consumption (Timing-aware P&R [27], [37])

Power Consumption (Fault tolerant-aware P&R)
Exploration space

acceptable solutions that meet performance specifications

Maximum affordable degradation in operation frequency

- Maximum Operation Frequency (Timing-aware P&R [27], [37])
- Maximum Operation Frequency (Fault tolerant-aware P&R)
- Power Consumption (Timing-aware P&R [27], [37])
- Power Consumption (Fault tolerant-aware P&R)
Exploration space

- Maximum Operation Frequency (Timing-aware P&R [27], [37])
- Maximum Operation Frequency (Fault tolerant-aware P&R)
- Power Consumption (Timing-aware P&R [27], [37])
- Power Consumption (Fault tolerant-aware P&R)

acceptable solutions that meet performance specifications

Maximum affordable degradation in operation frequency

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Exploration space

- Maximum Operation Frequency (Timing-aware P&R [27], [37])
- Maximum Operation Frequency (Fault tolerant-aware P&R)
- Power Consumption (Timing-aware P&R [27], [37])
- Power Consumption (Fault tolerant-aware P&R)

- Maximum affordable degradation in operation frequency

acceptable solutions that meet performance specifications
Exploration space

- Maximum Operation Frequency (Timing-aware P&R [27], [37])
- Maximum Operation Frequency (Fault tolerant-aware P&R)
- Power Consumption (Timing-aware P&R [27], [37])
- Power Consumption (Fault tolerant-aware P&R)

acceptable solutions that meet performance specifications

Maximum affordable degradation in operation frequency
### Number of sensitive bits

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Total number of config. Kbits</th>
<th>Sensitive configuration bits</th>
<th>Uniform TMR (based on [Xilinx2010])</th>
<th>Additional gain as compared to focused TMR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>No TMR</td>
<td>Focused TMR (W_{pOF} = 0.50, W_{EDP} = 0.50)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>No</td>
<td>Number</td>
<td>Improvement (%)</td>
</tr>
<tr>
<td>alu4</td>
<td>557.79</td>
<td>49.70</td>
<td>5.47</td>
<td>88.99%</td>
</tr>
<tr>
<td>apex2</td>
<td>724.17</td>
<td>92.69</td>
<td>6.33</td>
<td>93.17%</td>
</tr>
<tr>
<td>apex4</td>
<td>534.38</td>
<td>48.63</td>
<td>4.21</td>
<td>91.34%</td>
</tr>
<tr>
<td>bigkey</td>
<td>953.74</td>
<td>115.40</td>
<td>8.05</td>
<td>93.02%</td>
</tr>
<tr>
<td>clma</td>
<td>3,088.20</td>
<td>308.51</td>
<td>30.12</td>
<td>90.24%</td>
</tr>
<tr>
<td>des</td>
<td>1,287.21</td>
<td>171.71</td>
<td>11.49</td>
<td>93.31%</td>
</tr>
<tr>
<td>diffeq</td>
<td>508.84</td>
<td>63.45</td>
<td>5.67</td>
<td>91.06%</td>
</tr>
<tr>
<td>dsip</td>
<td>923.05</td>
<td>73.84</td>
<td>4.01</td>
<td>94.57%</td>
</tr>
<tr>
<td>elliptic</td>
<td>1,358.99</td>
<td>127.74</td>
<td>12.23</td>
<td>90.43%</td>
</tr>
<tr>
<td>ex1010</td>
<td>1,686.67</td>
<td>185.53</td>
<td>11.95</td>
<td>93.56%</td>
</tr>
<tr>
<td>ex5p</td>
<td>452.50</td>
<td>50.68</td>
<td>4.32</td>
<td>91.48%</td>
</tr>
<tr>
<td>frisc</td>
<td>1,434.38</td>
<td>154.91</td>
<td>15.44</td>
<td>90.03%</td>
</tr>
<tr>
<td>misex3</td>
<td>546.19</td>
<td>55.27</td>
<td>6.08</td>
<td>89.00%</td>
</tr>
<tr>
<td>pdc</td>
<td>2,023.79</td>
<td>287.18</td>
<td>20.97</td>
<td>92.70%</td>
</tr>
<tr>
<td>s208</td>
<td>662.35</td>
<td>75.51</td>
<td>3.67</td>
<td>95.14%</td>
</tr>
<tr>
<td>s38417</td>
<td>2,067.88</td>
<td>248.15</td>
<td>21.30</td>
<td>91.42%</td>
</tr>
<tr>
<td>s38584</td>
<td>2,119.48</td>
<td>254.34</td>
<td>19.09</td>
<td>92.49%</td>
</tr>
<tr>
<td>seq</td>
<td>680.89</td>
<td>75.37</td>
<td>6.38</td>
<td>91.54%</td>
</tr>
<tr>
<td>spla</td>
<td>1,520.26</td>
<td>163.43</td>
<td>12.90</td>
<td>92.11%</td>
</tr>
<tr>
<td>tseng</td>
<td>369.69</td>
<td>32.53</td>
<td>3.53</td>
<td>89.15%</td>
</tr>
<tr>
<td><strong>Average</strong>:</td>
<td></td>
<td>131.73</td>
<td>10.66</td>
<td>92%</td>
</tr>
</tbody>
</table>
## Experimental setup

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Number of LUTs</th>
<th>Array Size</th>
<th>Channel Width</th>
<th>Number of simultaneous games</th>
</tr>
</thead>
<tbody>
<tr>
<td>alu4</td>
<td>1,509</td>
<td>40 x 40</td>
<td>11</td>
<td>8</td>
</tr>
<tr>
<td>apex2</td>
<td>1,861</td>
<td>45 x 45</td>
<td>12</td>
<td>14</td>
</tr>
<tr>
<td>apex4</td>
<td>1,255</td>
<td>37 x 37</td>
<td>15</td>
<td>14</td>
</tr>
<tr>
<td>bigkey</td>
<td>1,817</td>
<td>55 x 55</td>
<td>8</td>
<td>5</td>
</tr>
<tr>
<td>clma</td>
<td>8,073</td>
<td>91 x 91</td>
<td>14</td>
<td>10</td>
</tr>
<tr>
<td>des</td>
<td>1,581</td>
<td>64 x 64</td>
<td>8</td>
<td>14</td>
</tr>
<tr>
<td>diffeq</td>
<td>1,475</td>
<td>40 x 40</td>
<td>8</td>
<td>9</td>
</tr>
<tr>
<td>dsip</td>
<td>1,370</td>
<td>55 x 55</td>
<td>7</td>
<td>11</td>
</tr>
<tr>
<td>elliptic</td>
<td>3,600</td>
<td>61 x 61</td>
<td>13</td>
<td>8</td>
</tr>
<tr>
<td>ex1010</td>
<td>4,545</td>
<td>69 x 69</td>
<td>12</td>
<td>5</td>
</tr>
<tr>
<td>ex5p</td>
<td>1,038</td>
<td>34 x 34</td>
<td>15</td>
<td>7</td>
</tr>
<tr>
<td>frisc</td>
<td>3,532</td>
<td>61 x 61</td>
<td>15</td>
<td>11</td>
</tr>
<tr>
<td>miscx3</td>
<td>1,376</td>
<td>39 x 39</td>
<td>12</td>
<td>8</td>
</tr>
<tr>
<td>pdc</td>
<td>4,506</td>
<td>69 x 69</td>
<td>19</td>
<td>9</td>
</tr>
<tr>
<td>s298</td>
<td>1,931</td>
<td>45 x 45</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>s38417</td>
<td>6,208</td>
<td>80 x 80</td>
<td>9</td>
<td>6</td>
</tr>
<tr>
<td>s38584</td>
<td>6,293</td>
<td>81 x 81</td>
<td>9</td>
<td>11</td>
</tr>
<tr>
<td>seq</td>
<td>1,733</td>
<td>43 x 43</td>
<td>13</td>
<td>7</td>
</tr>
<tr>
<td>spla</td>
<td>3,631</td>
<td>62 x 62</td>
<td>16</td>
<td>13</td>
</tr>
<tr>
<td>tseng</td>
<td>1,044</td>
<td>34 x 34</td>
<td>8</td>
<td>5</td>
</tr>
<tr>
<td><strong>Average:</strong></td>
<td><strong>2,918.9</strong></td>
<td><strong>56 x 56</strong></td>
<td><strong>11.65</strong></td>
<td><strong>9.15</strong></td>
</tr>
</tbody>
</table>
Execution cycles for identifying suspicious slices
### Number of slices that should be protected

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Number of slices that belong to regions of importance</th>
<th>Error (%)</th>
<th>Average players per game</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Based on power sources</td>
<td>Based on thermal profile</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Absolute (%)</td>
<td>Absolute (%)</td>
<td></td>
</tr>
<tr>
<td>alu4</td>
<td>392</td>
<td>26%</td>
<td>501</td>
</tr>
<tr>
<td>apex2</td>
<td>558</td>
<td>30%</td>
<td>739</td>
</tr>
<tr>
<td>apex4</td>
<td>351</td>
<td>28%</td>
<td>442</td>
</tr>
<tr>
<td>bigkey</td>
<td>799</td>
<td>44%</td>
<td>999</td>
</tr>
<tr>
<td>clma</td>
<td>2,203</td>
<td>27%</td>
<td>2,987</td>
</tr>
<tr>
<td>des</td>
<td>601</td>
<td>38%</td>
<td>727</td>
</tr>
<tr>
<td>diffeq</td>
<td>590</td>
<td>40%</td>
<td>635</td>
</tr>
<tr>
<td>dsip</td>
<td>425</td>
<td>31%</td>
<td>547</td>
</tr>
<tr>
<td>elliptic</td>
<td>1,620</td>
<td>45%</td>
<td>1,692</td>
</tr>
<tr>
<td>ex1010</td>
<td>1,591</td>
<td>35%</td>
<td>2,013</td>
</tr>
<tr>
<td>ex5p</td>
<td>311</td>
<td>30%</td>
<td>418</td>
</tr>
<tr>
<td>frisc</td>
<td>1,024</td>
<td>29%</td>
<td>1,272</td>
</tr>
<tr>
<td>misex3</td>
<td>537</td>
<td>39%</td>
<td>601</td>
</tr>
<tr>
<td>pdc</td>
<td>1,802</td>
<td>40%</td>
<td>1,955</td>
</tr>
<tr>
<td>s298</td>
<td>676</td>
<td>35%</td>
<td>731</td>
</tr>
<tr>
<td>s38417</td>
<td>2,732</td>
<td>44%</td>
<td>2,980</td>
</tr>
<tr>
<td>s38514</td>
<td>2,769</td>
<td>44%</td>
<td>3,147</td>
</tr>
<tr>
<td>seq</td>
<td>537</td>
<td>31%</td>
<td>712</td>
</tr>
<tr>
<td>spla</td>
<td>1,489</td>
<td>41%</td>
<td>1,561</td>
</tr>
<tr>
<td>tseng</td>
<td>418</td>
<td>40%</td>
<td>459</td>
</tr>
<tr>
<td><strong>Average</strong></td>
<td>1,071</td>
<td><strong>36%</strong></td>
<td><strong>1,256</strong></td>
</tr>
</tbody>
</table>
### Evaluation results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Initial (Without TMR)</th>
<th>Focused TMR (PoF = 0.50)</th>
<th>Uniform TMR (based on Xilinx2010)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Frequency (MHz)</td>
<td>Power (mWatt)</td>
<td>Frequency (MHz)</td>
</tr>
<tr>
<td>alu4</td>
<td>45.71</td>
<td>198.04</td>
<td>42.34</td>
</tr>
<tr>
<td>apex2</td>
<td>45.48</td>
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## Evaluation results

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*Delay improvement: 27%*

*Power improvement: 23%*
Conclusions

- A novel framework that support application implementation with fault-tolerance, is discussed
- Both at design-time, as well as run-time
- The methodology is applicable to commercial devices through the usage of Virtual FPGA platform
- The corrective action is immediate, since the faulty module never affects the circuit
- The conversion of a non-redundant system to a redundant one is easily undertaken without hardware modifications.
Thank you!

more info at ksiop@microlab.ntua.gr