

# Multi-wavelength Clock Recovery Based on a Fabry-Pérot filter and a Quantum-Dot Semiconductor Optical Amplifier

M. Spyropoulou, N. Pleros, G. Papadimitriou, I. Tomkos\*, A. Pomportsis

*Aristotle University of Thessaloniki, Department of Informatics, 54124 Thessaloniki, Greece*

*\* Athens Information Technology, 19.5Km Markopoulou Av., 19002 Peania-Athens, Greece*

*Tel: (+30) 2310 998776, Fax: (+30) 2310 998419, e-mail: [mspi@ait.edu.gr](mailto:mspi@ait.edu.gr), [npleros@csd.auth.gr](mailto:npleros@csd.auth.gr)*

## ABSTRACT

We present an all-optical multi-wavelength clock recovery circuit for operation with short optical data packets at 40 Gb/s and 160 Gb/s. The proposed scheme comprises a low-finesse Fabry-Perot Filter (FPF) followed by a Quantum-Dot Semiconductor Optical Amplifier (QD-SOA) and exploits the memory properties of the passive filtering element and the nonlinear gain characteristics of the homogeneously broadened spectral regions within the QD-SOA in order to acquire the clock signal of multiple incoming wavelengths on a per packet basis. Simulation-based performance analysis shows successful operation both at 40 Gb/s and 160 Gb/s with data packets at four wavelengths entering simultaneously the circuit, yielding a packet clock signal for every incoming data packet with only a few bits rise time and with significantly reduced timing jitter compared to the jitter of the original data.

**Keywords:** multi-wavelength optical clock recovery, Fabry-Pérot Filter, quantum-dot semiconductor optical amplifier.

## 1. INTRODUCTION

Wavelength Division Multiplexing (WDM) technology has been established as the main communication infrastructure for harnessing the huge bandwidth availability of optical fibers by enabling the simultaneous transmission of multiple wavelengths and utilizing every separate wavelength as a distinct high-speed information gateway. In WDM architectures, intra-node signal processing functionalities like clock extraction are performed separately for every incoming wavelength requiring a dedicated optical clock recovery module per lambda, increasing in this way the size, cost and complexity of the node. The realization of optical signal processing elements capable of acquiring synchronization with multiple incoming concurrent wavelengths has been heralded as the main-stream approach towards simplifying node architectures whilst retaining the attractive WDM capacity advantages, however, this scenario is accompanied by several limitations arising by the need for treating incoming wavelengths as independent entities. The operational framework of multi-wavelength clock extraction processes becomes even more challenging when entering the metro- and access-network domains, where the inherently packet-formatted traffic necessitates signal synchronization on a per packet basis with ultra-fast capture and decay times for the recovered packet clock signal.

So far, several techniques have been proposed for all-optical clock recovery, including phase-locked-loops [1] and mode-locked lasers [2], that require however long synchronization times prohibiting their operation with data packet traffic. Packet-per-packet timing extraction has been demonstrated by utilizing self-pulsating distributed feedback lasers (DFBs) [3] or, more recently, Fabry-Perot (FP) filter-assisted circuits followed by Semiconductor Optical Amplifier-based devices, paving the inroad towards more complex packet processing functionalities [4-5]. However, the response of the active optical elements employed also in these clock recovery modules is solely determined by the totally injected optical power impeding the isolated treatment of every separate wavelength. Multi-wavelength clock recovery operation has been presented only by means of purely passive optical circuitry using either FP resonators with high-Q filtering requirements [6] or bulky fiber-based configurations that exploit Talbot [7] and Brillouin scattering [8] effects in several kilometres of optical fiber.

In this paper, we present a novel scheme for high-rate multi-wavelength packet clock recovery comprising a low-finesse FPF tuned at the line-rate of the incoming signal and a QD-SOA. Clock extraction for data packets on the same wavelength is achieved by exploiting the memory properties of the FPF in order to transform each incoming packet into a clock resembling signal with intense amplitude modulation, whereas clock pulse amplitude equalization of this signal is obtained by utilizing the nonlinear gain characteristics of the QD-SOA that operates as a power limiting device. Its inhomogeneously broadened gain spectrum ( $\sim 100$  nm) encompasses several narrower homogeneously broadened regions due to the size distribution of the quantum-dots within the active region of the device, giving rise to almost independent carrier reservoirs constrained within the boundaries of a homogeneously broadened spectral region, thus enabling to accommodate the concurrent operation with data streams at multiple wavelengths. Performance analysis of the proposed circuit is presented based on numerical simulations, showing successful synchronization on a per packet basis with short data packets at four different wavelengths both at 40 Gb/s and 160 Gb/s and requiring only a small number of bits as clock rise and decay times. Timing jitter analysis reveals that the proposed technique yields recovered clock pulses with significantly reduced timing jitter compared to the respective value for the original data.

## 2. PRINCIPLE OF OPERATION

Figure 1 illustrates the setup of the multi-wavelength packet clock recovery unit. Four data packet streams at wavelengths  $\lambda_1$ ,  $\lambda_2$ ,  $\lambda_3$  and  $\lambda_4$  respectively are launched as common input signal into the clock recovery module that consists of a low finesse FPF followed by a QD-SOA.

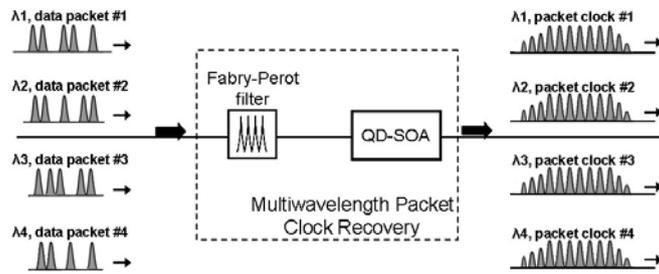


Figure 1. Multi-wavelength all-optical packet clock recovery unit.

Provided that the incoming wavelengths are located at the respective resonance peaks and that the data rate equals the free-spectral range (FSR) of the filter, the FPF partially fills the zeros of each incoming data stream with preceding ones at a repetition rate equal to the input bit rate yielding a clock resembling signal at its output for each respective input wavelength. This clock resembling signal has fast rise and decay times as a result of the low filter finesse and clock pulses with intense amplitude modulation. The QD-SOA is in turn used as an optical power limiting element in order to suppress the acquired amplitude modulation. Amplitude equalization can be accomplished only when the QD-SOA is operated under high saturation. At the non-linear regime, low peak power pulses will experience high gain and high peak power pulses will experience lower gain, respectively. Key feature of this technique is that clock acquisition is achieved within a small number of bits independently of the line rate and the derived clock signal. Multi-wavelength operation in QD-SOA materials relies on the confinement of each input wavelength within the homogeneous bandwidth of each quantum-dot group which lies under the heterogeneously broadened gain spectrum of the device and thus allows for separately treating the incoming wavelengths [9]. In order to provide spectral isolation, spacing of adjacent wavelengths should be at least larger than the QD-SOA homogeneous gain spectrum. In addition, QD-SOA based devices have shown great potential to operate at high bit rates due to their ultra-fast gain recovery time which lies in the sub-picosecond scale [10].

The performance analysis of this multi-wavelength clock recovery scheme is based on numerical simulations which use a model capable to describe the multi-wavelength functionality of the FPF and the carrier dynamics of the QD-SOA device [11]. The input data packet streams consist of 8 ps -first order Gaussian pulses at 40 Gb/s and 2 ps -first order Gaussian pulses at 160 Gb/s, modulated by a  $2^7-1$  PRBS bit pattern. The filter finesse is 30 and the QD-SOA is 3 mm long having small signal gain  $>35$  dB. The homogeneous bandwidth of the QD-SOA device is considered as small as 4 meV (equivalent to 4.96 nm at 1240 nm operation) which determined that the spectral spacing between adjacent wavelengths is 5.125 nm at 40 Gb/s and 5.74 nm at 160 Gb/s, taking into account that the filter FSR is 0.205 nm at 40 Gb/s and 0.82 nm at 160 Gb/s.

## 3. RESULTS AND DISCUSSION

The performance of the clock recovery scheme has been investigated both at 40 Gb/s and 160 Gb/s. In order to illustrate the principle of operation, it has been initially assumed that the four data packet streams have been modulated with the same PRBS bit pattern without suffering from timing jitter, which is shown in Figure 2(a) for the 40 Gb/s case and in Figure 3(a) for the 160 Gb/s case. The incoming data packets have been assumed to be 127-b long extracting the bits required for the rise and fall times of the acquired clock.

At 40 Gb/s, the peak power per input channel is -7 dBm resulting in a total average input power of -8.9 dBm. Figures 2(b) and 2(c) illustrate the pulse trace of the data stream at  $\lambda_2$  (denoted as ch2) at the output of the Fabry-Pérot filter and the QD-SOA at 40 Gb/s, respectively. It should be noted that, the four channels have shown similar performance and this is why only one out of four pulse traces is depicted here. After the FPF, the acquired amplitude modulation of the clock resembling signal is 4.5 dB, which is reduced after the QD-SOA to 1.48 dB, 1.40 dB, 1.46 dB and 1.30 dB for the data packet streams at  $\lambda_1$ ,  $\lambda_2$ ,  $\lambda_3$  and  $\lambda_4$ , respectively. In contrast to the amplitude equalization, the recovered clock signals suffer from extinction ratio degradation after passing through the QD-SOA due to the fact that it is operated under saturation. Indeed, the output extinction ratio of channels 1 and 4 is 7 dB whereas that of channels 2 and 3 is 6 dB. This is attributed to the fact that the four channels are closely and equally spaced around the centre of the inhomogeneously broadened gain spectrum of the QD-SOA and the zero-level of the inner channels encounters larger gain than the outer ones.

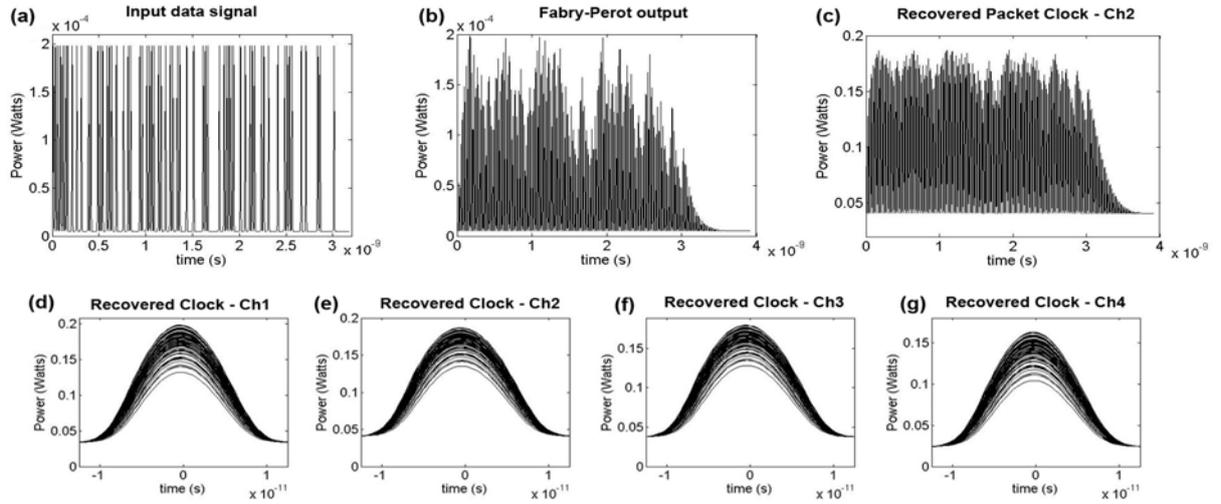


Figure 2. 40 Gb/s: (a) Input data pulse-trace (b) FPF output pulse trace (c) QD-SOA output pulse-trace for ch2 (d-g) eye diagrams of the recovered clock signals.

The same analysis follows at 160 Gb/s. Figure 3 illustrates the pulse traces of the (a) incoming data packet (b) FPF output and (c) recovered packet clock for data packet at  $\lambda_2$ . The peak power per input channel is now  $-3$  dBm resulting in an average input power of  $-4.92$  dBm. At the output of the FPF the clock-resembling signal suffers from amplitude modulation of  $5.2$  dB. Figure 3(c) illustrates that the zero-level of the QD-SOA output pulse trace reaches a steady level after the first 6 bits indicating the time interval that the QD-SOA gain needs to reach its maximum value. Figures 3(d-g) illustrate the eye diagrams of the recovered clock signals. The remaining amplitude modulation of the recovered clock pulses is  $1.28$  dB,  $1.11$  dB,  $1.16$  dB and  $1.71$  dB for channels 1-4, respectively. Furthermore, it is noteworthy that the recovered eye diagrams show an overshooting at the leading edge of the pulses which is related to the fact that the leading edge saturates the amplifier resulting in the trailing edge to experience less gain [12]. This effect is evident at 160 Gb/s because the duration of the pulse is comparable to the gain recovery time of the active device ( $\sim 2$  ps). Finally, the amplitude modulation suppression is better for the 160 Gb/s case with respect to the 40 Gb/s case. This may be attributed to the ultra-fast carrier dynamics of QD-SOAs.

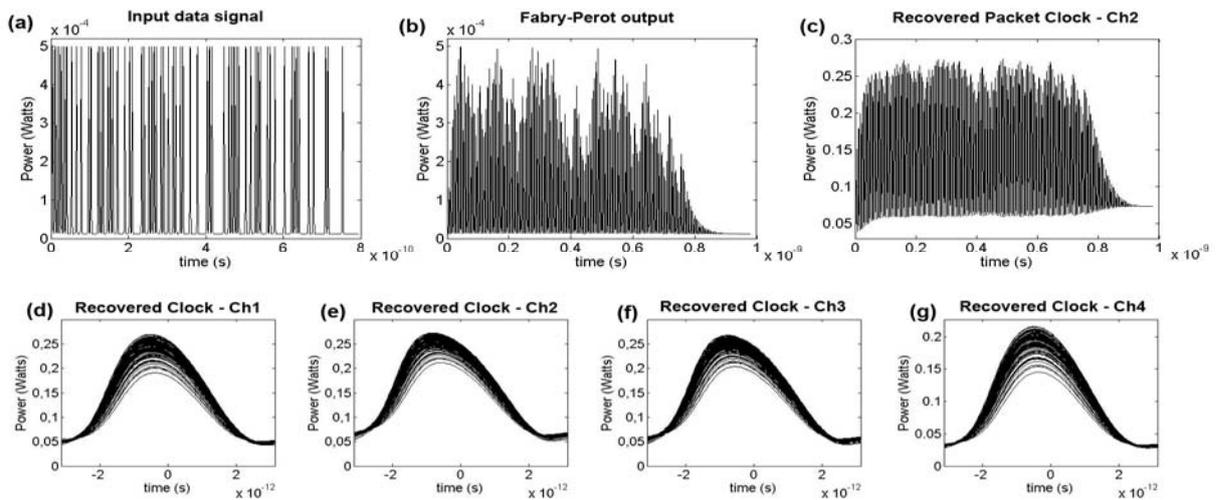


Figure 2. 160 Gb/s: (a) Input data pulse-trace (b) FPF output pulse trace (c) QD-SOA output pulse-trace for ch2 (d-g) eye diagrams of the recovered clock signals.

The following results illustrate the performance of the multi-wavelength clock recovery unit at the presence of input jitter. Figures 4(d) and 4(h) present the root mean square (rms) value of the output versus the input jitter. The diagonal stripe represents the  $y = x$  function which indicates that the output rms jitter is equal to the input value. It is noteworthy that at both bit rates, the output data pulses have acquired a clock with reduced timing jitter up to 80 % at both bit rates.

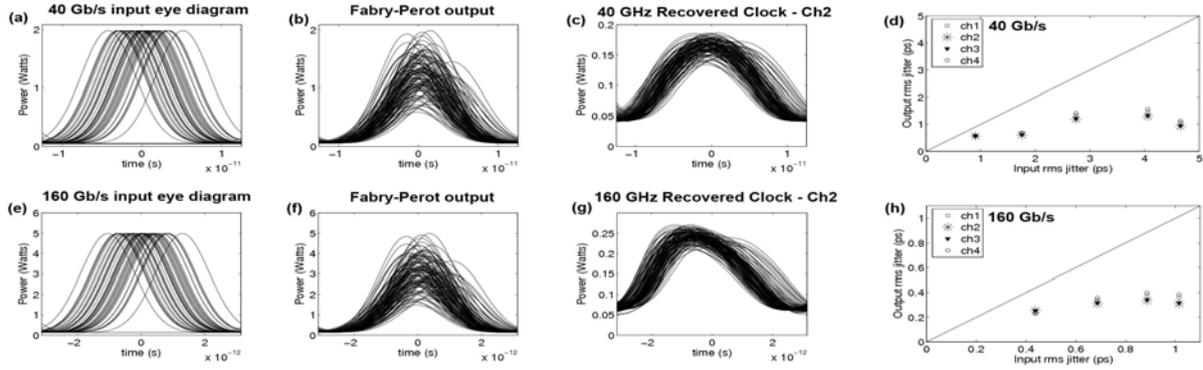


Figure 4. Eye diagrams at the input, FPF output and QD-SOA output for ch2 at (a-c) 40 Gb/s and (e-g) 160 Gb/s. Output versus input rms jitter for ch1-ch4 at (d) 40 Gb/s and (h) 160 Gb/s.

Figures 4(a) and 4(b) illustrate the eye diagrams of the input data packet stream at  $\lambda_2$ , suffering from rms jitter 1.76 ps and 0.44 ps which comprise approximately one fourth of the pulse width at 40 Gb/s and 160 Gb/s, respectively. After passing through the FPF the pulses have been almost fully synchronized having output rms timing jitter reduced by 65 % at 40 Gb/s and by 41 % at 160 Gb/s, respectively. The filtering function of the FPF removes the timing jitter but induces spectral broadening of the pulses. In particular, at 40 Gb/s the pulse width has increased from 8 ps to 12 ps and at 160 Gb/s the pulse width has increased from 2 ps to 3 ps. Finally, after equalization of the amplitude discontinuities through the QD-SOA, the remaining amplitude modulation of the recovered clock pulses at 40 Gb/s is 1.4 dB indicating a suppression of 69 % whereas, the amplitude modulation of the recovered data pulses at 160 Gb/s is 1.2 dB indicating a suppression of 77 %.

#### 4. CONCLUSIONS

In this paper, we have numerically investigated the performance of an all-optical multi-wavelength clock recovery unit based on a Fabry-Pérot Filter and a quantum-dot semiconductor optical amplifier for four incoming data packet streams, in terms of amplitude modulation suppression of the clock resembling signals and timing jitter reduction of the recovered clock signals. Similar performance has been demonstrated for all data packet streams, highlighting the potential of this scheme to treat each input wavelength independently and provide high bit rate multi-wavelength all-optical clock recovery in future WDM networks.

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